



Docket No.: 067161-0086

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of	:	Customer Number: 20277
Koichi ISHIMI	:	Confirmation Number: 1807
Application No.: 10/646,823	:	Group Art Unit: 2816
Filed: August 25, 2003	:	Examiner: Hail Nguyen

For: INFORMATION PROCESSING APPARATUS WITH CLOCK GENERATING CIRCUIT  
AND INFORMATION PROCESSING APPARATUS WITH CLOCK DELAYING CIRCUIT

**COMMENTS ON REASONS FOR ALLOWANCE**

Mail Stop Issue Fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

The Notice of Allowability, dated April 20, 2005, presents a statement of reasons for allowance at paragraph 3. It is respectfully submitted that this paragraph contains inaccuracies, as described below.

The phrase “for generating . . . of the clock signal” at page 3, lines 8-10, of the Notice of Allowability has been read as being performed by the “first counter (32)” at line 5. However, this function should be attributed to the “clock generating circuit (10)” in line 3, or the “multiplication circuit (20)” in line 5.

In addition, the statement that the clock signal (DL-OUT) is determined by an initial value is not accurate. The attribution of the “first initial count value” to the label “/WL” at page

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3, line 7, is also inaccurate. "/WL" is not a first initial count value, but a delay signal that is output from the digital counter 32 corresponding to the "first counter (32)".

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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**Date: June 29, 2005**  
GZR/lmn

**Please recognize our Customer No. 20277  
as our correspondence address.**

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